

**ABSTRACT****DIGITAL SIGNAL PROCESSOR**

A digital signal processor architecture allows the digital signal processor to be used  
5 efficiently for multiplying words which are longer than the word length for which the  
architecture is primarily designed. The multiplication unit has a register file which is  
adapted to store data words of a first length, and a multiplier which is adapted to  
multiply together data words of a second length, the second length being twice the first  
length. In a first mode, the architecture multiplies data words of the first length, by  
10 extending them to the second length. In a second mode, the architecture multiplies  
data words of the second length, by retrieving each of the data words in two parts,  
each part being of the first length.